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EXAMINER	
LEE, SHUN K	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 05/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/833,363	BOIERIU ET AL.	
	Examiner	Art Unit	
	Shun Lee	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 04 November 2002 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on 4 November 2002. These drawings are not acceptable.

2. The corrected or substitute drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because:

(a) reference character "1" has been used to designate both CdTe thin films (*e.g.*, pg. 17, line 14) and ROIC (*e.g.*, pg. 18, line 12);

(b) reference character "2" has been used to designate both Si (*e.g.*, pg. 17, line 13) and metal pads (*e.g.*, pg. 18, line 11);

(c) reference character "3" has been used to designate both substrate (*e.g.*, pg. 17, line 15) and ROIC pads (*e.g.*, pg. 21, line 15);

(d) reference character "4" has been used to designate both HgCdTe (*e.g.*, pg. 17, line 16) and encapsulant layer (*e.g.*, pg. 23, line 21);

(e) reference character "5" has been used to designate both Si (*e.g.*, pg. 17, line 20) and ROIC common (*e.g.*, pg. 22, line 3);

(f) reference character "6" has been used to designate both buffer layer (*e.g.*, pg. 17, lines 19-20) and growth window (*e.g.*, pg. 20, line 23);

(g) reference character "7" has been used to designate both HgCdTe (*e.g.*, pg. 17, line 20) and CdTe buffer layer (*e.g.*, pg. 23, line 20);

(h) reference character "26" has been used to designate: MIS device (*e.g.*, pg. 9, line 7), detector outputs (*e.g.*, pg. 21, line 21), detectors (*e.g.*, pg. 22, line 7), and gold metal (*e.g.*, pg. 30, lines 8-9);

(i) reference character "27" has been used to designate both detectors (*e.g.*, pg. 22, line 9) and gold metal (*e.g.*, pg. 30, lines 8-9);

(k) reference character "32" has been used to designate: first HgCdTe narrow band gap layer (*e.g.*, pg. 7, line 20), wider band gap p-HgCdTe layer (*e.g.*, pg. 8, line 10), and narrow band gap p-type HgCdTe infrared absorber layer (*e.g.*, pg. 8, lines 21-22);

(l) reference character "33" has been used to designate: second HgCdTe wider band gap layer (*e.g.*, pg. 7, line 20), first p-HgCdTe narrow band gap layer (*e.g.*, pg. 8, line 9), and wider band gap p-type HgCdTe layer (*e.g.*, pg. 8, lines 20-21);

(m) reference character "34" has been used to designate both photodiode (*e.g.*, pg. 7, line 21 or pg. 8, line 10) and n-type light receiving region (*e.g.*, pg. 8, lines 22-23);

(n) reference character "37-39" has been used to designate: signal processing circuits 37-39 (*e.g.*, pg. 9, line 16), drain diode 37 (*e.g.*, pg. 8, line 11), source diode 38 (*e.g.*, pg. 8, line 11), and insulating layer 39 (*e.g.*, pg. 8, line 15); and

(o) reference character "40" has been used to designate both insulating film (*e.g.*, pg. 8, line 2) and Metal Insulator Semiconductor (MIS) switch (*e.g.*, pg. 8, line 14).

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The corrected or substitute drawings are also objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 49, 50, and 53 (Fig. 18). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. Figures 9a and 9b should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (pg. 15, line 16). See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities:

(a) on pg. 1, related application number is missing (an application for a patent when filed may incorporate "essential material" by reference to (1) a U.S. patent, (2) a U.S. patent application publication, or (3) a pending U.S. application, subject to certain conditions, see MPEP §608.01(p); and the guidelines for situations where applicant is permitted to fill in a number for Application No. _____ left blank

in the application as filed can be found in *In re Fouche*, 439 F.2d 1237, 169 USPQ 429 (CCPA 1971));

(b) on pg. 1, "carries" in line 10 should probably be --carriers--; and

(c) on pg. 8, "window 34" in line 6 should probably be --photodiode 34--.

Appropriate correction is required.

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

7. Claims 4, 5, 8, and 11-13 are objected to because of the following informalities:

(a) in claim 4, "said readout input cell" (there is insufficient antecedent basis for this limitation in the claim) on line 2 should probably be --a first input of said readout integrated circuit-- (which also provides antecedent basis for "said first input" on line 6);

(b) in claim 4, "said readout common cell" (there is insufficient antecedent basis for this limitation in the claim) on line 3 should probably be --a common input of said readout integrated circuit--;

(c) in claim 4, "a detector output" on line 2 should probably be --a detector output of said photovoltaic infrared detecting cell--;

(d) in claim 4, "a detector common" on line 2 should probably be --a detector common of said photovoltaic infrared detecting cell--;

(e) in claim 5, "said sloped side" (there is insufficient antecedent basis for this limitation in the claim) on line 1 should probably be --a sloped side--;

(f) in claim 8, "claim 6" on line 1 should probably be --claim 7-- in order to provide antecedent basis for "said first n-type HgCdTe layer" on line 3 of claim 8;

(g) "signal input gates" on line 8 of claim 11 and again on line 10 of claim 11 is indefinite and can lead to misinterpretation (if the two elements are different, the former should be identified as --first signal input gate-- and the later should be identified as --second signal input gate--);

(h) in claim 12, "dyhdride" on line 3 should probably be --dihydride--;

(i) in claim 12, "degrees C" on line 7 should probably be --°C--;

(j) in claim 12, "degrees C" on line 10 should probably be --°C--;

(k) in claim 12, "degrees C" on line 13 should probably be --°C--;

(l) in claim 13, "H_20" on line 2 should probably be --H_2O--; and

(m) in claim 13, "a dyhdride" on line 4 should probably be --said dihydride--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it

pertains, or with which it is most nearly connected, to make and/or use the invention. The specification discloses (pg. 21, lines 4-11) that a concentrated NH_4F (20%-40%) is used. However, there was no disclosure of the composition of the concentrated NH_4F etchant. Further, the specification fails to disclose temperature at which the two-step etch process occur. Thus claim 13 contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: a horizontal plane to other elements in the claim (*e.g.*, said face of said semiconductor substrate). It is suggested that "a horizontal plane" should probably be "said face of said semiconductor substrate" (see pg. 29, lines 3-5).

12. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 13 recites the limitation "the Si wafer" in lines 2 and 4. There is insufficient antecedent basis for this limitation in the claim. Claim 13 also recites the limitation "the passivation layer" in line 2. There is insufficient antecedent basis for this limitation in the claim.

13. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 14 recites the limitation "the entire sample" in line 14. There is insufficient antecedent basis for this limitation in the claim.

Further, claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: a horizontal plane to other elements in the claim (*e.g.*, said face of said semiconductor substrate). It is suggested that "a horizontal plane" should probably be "said Si(001) surface" (see pg. 29, lines 3-5).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

16. Claims 1, 3, 6, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Tew *et al.* (US 4,686,373), Zanio *et al.* (US 4,910,154), and Goodwin (incorporated by reference US 5,300,777).

In regard to claim **10**, Bevan *et al.* (and US 5,300,777 which is incorporated by reference in lines 9 and 10 on column 5) disclose (Figs. 6-8) an infrared sensing device having at least one infrared light sensitive element (photodiode 30 or array 24; column 4, line 62 to column 5, line 7), comprising: a readout integrated circuit (20) formed at a face of a semiconductor layer (12) having a tilt of approximately one degree from the (100) crystal direction (*i.e.*, nominal (100) lattice orientation; column 3, lines 9-12); at least one infrared light sensitive element (30 or 24) formed on a first surface of said readout integrated circuit (20), said at least one infrared light sensitive element (30 or 24) including:

(a) buffer layer (14a, 14b, 14c, 16) such as CdTe;

(b) a first layer (18a) of Group II-VI semiconductor material (*e.g.*, HgCdTe) on said buffer layer (14a, 14b, 14c, 16), said first layer (18a) of Group II-VI semiconductor material having a first band gap;

(c) said buffer layer (14a, 14b, 14c, 16) functionally reducing mismatch (column 2, lines 22-29) between said readout integrated circuit (20) and said first layer(18a) of Group II-VI semiconductor material;

(d) a second layer (18b) of Group II-VI semiconductor material (*e.g.*, HgCdTe) disposed on said first layer (18a) of Group II-VI semiconductor material, said second layer (18b) of Group II-VI semiconductor material having a second band gap; and

(e) said first band gap being different (*e.g.*, smaller; incorporated by reference US 5,300,777 column 2, line 62 to column 3, line 1) from said second band gap.

The infrared sensing device of Bevan *et al.* lacks that the at least one infrared light sensitive element (30 or 24) is a mesa. However, infrared light sensitive element as a mesa is well known in the art. For example, Tew *et al.* teach (column 8, lines 44-51) that the infrared light sensitive element is a mesa (120 in Fig. 17). As another example, Zanio *et al.* teach (column 8, lines 44-51) that the infrared light sensitive element is a mesa (14 in Fig. 1 or 24 in Fig. 2) having a height of ~15 μm. As still another example, Goodwin teaches (column 4, lines 44-51) that the infrared light sensitive element is a mesa. Therefore it would have been obvious to one having ordinary skill in the art that the at least one infrared light sensitive element in the infrared sensing device of Bevan *et al.* is a conventional mesa having a height of about 15 μm.

In regard to claim **11** which is dependent on claim 10, Bevan *et al.* also disclose (Figs. 6-8) a first cell and a second cell not overlapping the first cell (*i.e.*, an infrared detecting array of p-n junction diodes; column 4, line 62 to column 5, line 7) at least partially extending into said first layer of Group II-VI semiconductor material where first and second conductive interconnect traces (32 or equivalently 24 and 26; column 5, lines 46-48) are formed between the infrared detecting cells (30) and signal input gates

of said readout circuit (20) and that the conductive interconnect traces monolithically connect the infrared detecting cells lying in one plane to the readout integrated circuits lying in another plane. The infrared sensing device of Bevan *et al.* lacks that the first and second conductive interconnect trace running over a first and second sloped side of the mesa, respectively. Tew *et al.* teach (column 8, lines 44-51; Fig. 17) that connection of n-type regions 114 of an active device mesa 120 to an aluminum pad on the silicon occurs through a via 122 located adjacent to the active device mesa 120. Therefore it would have been obvious to one having ordinary skill in the art to provide first and second conductive interconnect trace running over a first and second sloped side of a conventional mesa having a height of about 15 μm in the infrared sensing device of Bevan *et al.*, in order to connect first and second cells of the infrared detecting array to readout circuit signal input gates which are located adjacent to the mesa.

In regard to claims **1** and **3**, Bevan *et al.* in view of Tew *et al.*, Zanio *et al.*, and Goodwin is applied as in claim 11 above.

In regard to claim **6**, Bevan *et al.* in view of Tew *et al.* (US 4,686,373), Zanio *et al.*, and Goodwin is applied as in claim 11 above for rows of infrared detecting cells and rows of signal input gates of said readout circuit.

17. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Tew *et al.* (US 4,686,373), Zanio *et al.* (US 4,910,154), and Goodwin (incorporated by reference US 5,300,777) as applied to claim 1 above, and further in view of Chapman *et al.* (US 5,581,084).

In regard to claim **2** (which is dependent on claim 1) and claim **4** (which is dependent on claim 1), Bevan *et al.* in view of Tew *et al.*, Zanio *et al.*, and Goodwin is applied as in claim 11 above. The modified infrared sensing device of Bevan *et al.* lacks that the infrared detecting cell has a common contact which is conductively connected a common contact of the readout integrated circuit. Infrared detecting cells are well known in the art. For example, Chapman *et al.* teach (Fig. 6) that infrared detecting cells have a common anode contact which is conductively connected a common contact of the readout integrated circuit. Therefore it would have been obvious to one having ordinary skill in the art to connect the common anode contact of two color infrared detecting cells in the modified infrared sensing device of Bevan *et al.* to the readout integrated circuit, in order to detect infrared in two wavelength bands as taught by Chapman *et al.*

18. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Tew *et al.* (US 4,686,373), Zanio *et al.* (US 4,910,154), and Goodwin (incorporated by reference US 5,300,777) as applied to claim 3 above, and further in view of Bean *et al.* (US 3,936,929).

In regard to claim **5** which is dependent on claim 3, the modified infrared sensing device of Bevan *et al.* lacks that a sloped side of said mesa has a slope angle between about 40 and 50 degrees relative to the mesa base. Mesas are well known structures. For example, Bean *et al.* teach (column 4, lines 16-30) mesas formed in (100) crystal orientation material have well known slopes of 46° or 54° and that metallic interconnects formed on these mesa slopes allow dependable electrical connection. Therefore it

would have been obvious to one having ordinary skill in the art to provide a mesa slope angle between about 40 and 50 degrees in the modified infrared sensing device of Bevan *et al.*, in order to form dependable electrical connections as taught by Bean *et al.*

19. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Tew *et al.* (US 4,686,373), Zanio *et al.* (US 4,910,154), and Goodwin (incorporated by reference US 5,300,777) as applied to claim 6 above, and further in view of Koehler (US 4,137,544).

In regard to claims **7-9** which are dependent on claim 6, the modified infrared sensing device of Bevan *et al.* lacks that the infrared detecting cells include an arsenic compound at least partially extending into the first layer of Group II-VI semiconductor material wherein both the first and second layers of Group II-VI semiconductor material are formed of indium doped n-type HgCdTe. Infrared detecting cells are well known in the art. For example, Koehler teaches (Fig. 1) that the infrared detecting cells include an arsenic compound (14; column 3, lines 55-61) at least partially extending into the first layer (10) of Group II-VI semiconductor material wherein both the first (10) and second (12) layers of Group II-VI semiconductor material are formed of n-type HgCdTe in order to provide an accumulation layer which prevents the natural inversion of n-type HgCdTe (column 4, lines 26-29). Koehler also teaches (column 4, lines 31-36) that n-type HgCdTe can be formed by ion implantation or diffusion of donor impurities such as indium. Therefore it would have been obvious to one having ordinary skill in the art to provide two layers of indium doped n-type HgCdTe and to form pn junction by implanting an arsenic compound in the modified infrared sensing device of Bevan *et al.*,

in order achieve a desired detectivity in the 8-14 μm wavelength region as taught by Koehler (column 2, lines 53-60).

20. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Goodwin (incorporated by reference US 5,300,777), de Lyon (US 5,306,386), and Wu *et al.* (US 6,043,141).

In regard to claim **12**, Bevan *et al.* is applied as in claims 10 and 11 above. The method of Bevan *et al.* lacks inserting the read-out integrated circuit having a passivated and clean Si (001) surface (*i.e.*, dihydride terminated smooth surface by etching) into an MBE chamber for depositing the buffer layer, first layer, and the second layer in sequence on the Si (001) surface while maintaining the read-out integrated circuit at a temperature less than 500°C. MBE are well known in the art. For example, Bevan *et al.* teach (column 1, lines 10-61) it is known in the art to deposit a CdTe buffer layer and a HgCdTe layer on a Si (001) surface by MBE. As another example, de Lyon teaches (column 3, line 54 to column 4, line 54) to deposit a CdTe buffer layer and a plurality of layers on a Si (001) surface by MBE. As still another example, Wu *et al.* teach (column 5, lines 60-67) to deposit HgCdTe layers on a semiconductor surface by the MBE (which is the typical method of in situ growth of high quality HgCdTe epilayers having abrupt heterojunctions in a single growth run; column 1, lines 19-31) at a temperature less than 500°C preferably in a range of 155 to 165°C. Therefore it would have been obvious to one having ordinary skill in the art to MBE deposit a CdTe buffer layer followed by first and second HgCdTe layers on a Si (001) surface at a temperature

less than 500°C in the method of Bevan *et al.*, in order obtain abrupt heterojunctions in a single growth run.

21. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bevan *et al.* (US 5,838,053) in view of Goodwin (incorporated by reference US 5,300,777), de Lyon (US 5,306,386), and Wu *et al.* (US 6,043,141) as applied to claim 12 above, and further in view of La Chapelle, Jr. (US 5,366,934), McConnell *et al.* (US 4,778,532), Hetrick *et al.* (US 6,096,149), Kaganowicz *et al.* (US 4,705,760), Norimatsu *et al.* (US 6,049,638), Tew *et al.* (US 4,686,373), and Koehler (US 4,137,544).

In regard to claims **13-15** which are dependent on claim 12, the method of Bevan *et al.* lacks a detailed description of the semiconductor process techniques (*i.e.*, removing a passivation layer by etching with a diluted solution of $HF:H_2O$ and forming the dihydride terminated smooth Si(001) surface by etching with a concentrated solution of NH_4F; depositing a thin CdTe cap layer on the second HgCdTe layer; coating the entire structure with a photoresist; selectively opening a plurality of windows in the photoresist; fabricating a plurality of p-n junctions by implementing arsenic atoms through the windows selectively by ion implantation technique; annealing the ROIC to activate the arsenic; removing the masking photoresist layer; selectively protecting the grown infrared material structure with a photoresist while leaving the remaining areas uncovered; etching the uncovered areas to expose the ROIC contact pads; selectively protecting the grown infrared material structure with a photoresist, leaving the rest of the areas open; and forming a 40-50° side wall slope mesa structure by etching with an

etching solution such as 4% bromine in hydrobromic acid solution) used to fabricate the infrared sensing device. However, semiconductor process techniques such as passivation layers, photoresist masks, selective etching, and selective ion implantation are well known in the art. For example, La Chapelle, Jr. teaches (column 1, lines 18-66) it is well known in the art to provide a passivation layer in order to enhance and preserve the best detector properties. As another example, McConnell *et al.* teach (column 5, line 39 to column 6, line 14) etchants comprising HF are well known in the art; Hetrick *et al.* (column 1, line 64 to column 2, line 2) and Kaganowicz *et al.* (column 2, lines 59-68) teach etchants comprising NH_4F are well known in the art; and Norimatsu *et al.* teach (column 4, lines 56-63) that wet etching can be performed with an etchant comprising bromine in hydrobromic acid. As still another example, Tew *et al.* teach (column 5, lines 21-33) to provide a photoresist mask for selective etching and Koehler teaches (column 3, lines 43-61) to provide a mask for selective ion implantation. Therefore it would have been obvious to one having ordinary skill in the art to use standard semiconductor processing techniques in the modified method Bevan *et al.* in order to form the infrared sensing device.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shun Lee whose telephone number is (703) 308-4860. The examiner can normally be reached on Tuesday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (703) 308-4852. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

CONSTANTINE HANNAHER
PRIMARY EXAMINER
GROUP ART UNIT 2878

SL
May 9, 2003